REMARKS

This Amendment is filed in response to the final Office Action dated November 4, 2004, which has a shortened statutory period set to expire February 4, 2004.

Applicants Address Claim Objections

The Office Action states that the "specification fails to clearly specify the number of the scan chains, so as to enable a person skilled in the art to calculate a range for the scan chains 'wherein the number of said scan chains can be greater than one and less than a maximum number'". Applicants respectfully disagree. This remark highlights an important advantage of Applicants' invention. That is, the number and length of the scan chains in a design under test can be configured for use with different testers. Because the number and length of the scan chains can be configured, an exact number of scan chains should not be required in the broadest claims. The Specification provides support for above limitation.

For example, Applicants direct the Examiner's attention to Figures 4A and 4B, which illustrate exemplary devices under test.

In Figure 4A, two modes of operation are supported, high performance and low performance. Specification, page 18, lines 1-15. In a high performance mode (selector 270a is low), scan chains 310a and 310b receive inputs from scan inputs 320a and 320b, respectively, and scan data out using scan outputs 340a and 340b, respectively. In contrast, in a low performance mode (selector 270a is high), scan input 320a and scan output 340b are ignored. Specification, page 19, lines 10-12. Thus, two scan chains independently function in the high performance mode whereas only one scan chain (scan chains 310a and 310b connected in series) functions in the low performance mode. This

configuration is scalable, wherein for a typical implementation, the scan and mux circuitry would be replicated many times over with all muxes having their select lines coupled together to provide the performance adjustments. Specification, page 20, lines 4-9.

In Figure 4B, three modes of operation are supported, high performance, medium performance, and low performance. Specification, page 20, lines 11-21. In a high performance mode, there are four separate scan chains (310a, 310b, 310c, and 310d). In a medium performance mode, there are two separate scan chains (chain 310a + 310b, chain 310c + 310d). In a low performance, there is a single scan chain (chain 310a + 310b + 310c + 310d). This configuration is also scalable, wherein for a typical implementation, the configuration of Figure 4B can be replicated many times over with common muxes having the same control lines coupled thereto. Specification, page 20, lines 19-21.

By providing the appropriate configuration logic (e.g. scan and multiplexer circuitry), a design under test can be configured to provide N scan chains, wherein N can be greater than one and less than a maximum number of scan chains. Therefore, the maximum number of scan chains is not an arbitrary number as characterized in the Office Action.

Based on the above remarks, Applicants request reconsideration and withdrawal of the objection to Claims 1-29.

Claims 1-29 Are Patentable Over Motika and Omura

Claim 1 recites in part:

> reconfiguration logic coupled to said scan chains and for altering the number of pins required to test said device under test by reconfiguring the individual length and number of said scan chains based on a mode signal, wherein the number of said scan chains can be greater

than one and less than a maximum number of scan chains, said reconfiguration logic providing compatibility between said test vectors and said second tester having said second pin capacity, said mode signal selecting between said first tester and said second tester.

Claim 8 recites in part:

reconfiguration logic coupled to said scan chains and for altering the number of pins required to test said device under test by reconfiguring the individual length and number of said scan chains based on said user selector, wherein the number of said scan chains can be greater than one and less than a maximum number of scan chains, said reconfiguration logic providing compatibility between said test vectors and said tester having said second pin capacity.

Claim 15 recites in part:

reconfiguration logic coupled to said scan chains and for altering the number of pins required to test said device under test by reconfiguring the individual length and number of said scan chains based on said test mode, wherein the number of said scan chains can be greater than one and less than a maximum number of scan chains, said reconfiguration logic providing compatibility between said test vectors and said tester having said low pin capacity.

Claim 22 recites in part:

c) in response to said step b), altering the number of pins required to test said device under test by reconfiguring the individual length and number of scan chains internal to said device based on said test mode, wherein the number of said scan chains can be greater than one and less than a maximum number of scan chains, wherein said altering provides compatibility between said test vectors and said tester having said second pin capacity.

As taught by Applicants, configurations of the design may include different pin counts and requirements from the tester.

Specification, page 18, lines 4-6. In one configuration, a high pin count is used including individual functional inputs and many balanced scan chains for low test application time. Specification, page 18, lines 7-9. In another configuration, a very low pin count can be achieved at the trade-off of higher test application times caused by longer scan chains. A user-adjustable test mode selector allows reconfiguration of the on-chip circuitry, thereby ensuring compatibility with testers of different pin capacities. Specification, page 16, lines 4-11. Notably, Applicants' invention can make full use of the various different types of testers that a test facility has but uses a single set of developed test vectors. Specification, page 6, lines 2-4.

Motika fails to disclose or suggest this limitation and its advantages. For example, Motika teaches that a mode select signal allows for normal LSSD or WRPLBIST test modes. Col. 5, lines 51-53. Thus, referring to Fig. 2 of Motika, in the LSSD mode, the multiplexers are set to essentially form one serpentine scan chain having a length of all the scan chains (i.e. forming a single scan chain). In contrast, in the WRPLBIST test mode, the multiplexers are set to provide weighted random patterns (WRPs) to each of the scan chains. Thus, the number of scan chains in this mode is equal to the maximum number of scan chains.

In general, Motika teaches test methodologies that allow for three distinct test modes. Col. 2, lines 48-49. In a first mode based on deterministic LSSD and test techniques described in U.S. Patent 3,783,254, the test supplies the patterns to be loaded in each SRL (shift register latch) chain and then pulses the appropriate system clocks. Col. 2, lines 52-55. In a second mode based on WRP (weighted random pattern) methodology, an LFSR (linear feedback shift register) algorithmically

generates a set of pseudo random test patterns at the tester. Col. 2, lines 58-63. These patterns are then weighted to optimize them for a specific logic design. Col. 2, lines 63-64. In a third mode, some of these techniques can be extended to BIST (built in self test) and incorporates the LFSR and a MISR (multiple input signature register) in the DUT. Col. 3, lines 3-5. Motika attempts to balance these three test modes. Col. 3, lines 10-13.

Fundamentally speaking, the recited device/method/system, ties patterns to configurations in such a way that the same test patterns can be executed through different interfaces. In contrast, Motika's teaching applies different patterns and test methodologies implemented on the same design, which has nothing to do with efficiency of applying the same tests for efficient utilization of ATE resources. Therefore, in particular, Motika fails to disclose or suggest compatibility between said test vectors as well as the reconfiguration logic for altering the number of pins required to test the DUT by reconfiguring the individual length and number of said scan chains based on the test mode, wherein the number of scan chains can be greater than one and less than a maximum number of scan chains.

Omura fails to remedy the deficiencies of Motika. Specifically, Omura teaches providing a BIST (built in self test) in a semiconductor device having a memory circuit and in a semiconductor test apparatus including a power supply for applying a power supply voltage to the semiconductor device, an instructing circuit for instructing execution of a test and output of data indicative of the test result to the self test circuit, and a receiving circuit for receiving data output from the self test circuit. Col. 2, lines 30-39. According to Omura, this configuration reduces the number of terminals for signal output and the number of pattern generators and increases

the number of semiconductor devices that can be tested on one time per one semiconductor testing apparatus. Col. 2, lines 39-46. Therefore, Omura also fails to disclose or suggest compatibility between said test vectors as well as the reconfiguration logic for altering the number of pins required to test the DUT by reconfiguring the individual length and number of said scan chains based on the test mode, wherein the number of scan chains can be greater than one and less than a maximum number of scan chains.

Because Motika and Omura fail to disclose or suggest the recited limitations, much less their advantages, Applicants request reconsideration and withdrawal of the rejection of Claims 1, 8, 15, and 22.

Claims 2-7 depend from Claim 1 and therefore are patentable for at least the reasons provided for Claim 1. Based on those reasons, Applicants request reconsideration and withdrawal of the rejection of Claims 2-7.

Claims 9-14 depend from Claim 8 and therefore are patentable for at least the reasons provided for Claim 8. Based on those reasons, Applicants request reconsideration and withdrawal of the rejection of Claims 9-14.

Claims 16-21 depend from Claim 15 and therefore are patentable for at least the reasons provided for Claim 15. Based on those reasons, Applicants request reconsideration and withdrawal of the rejection of Claims 16-21.

Claims 23-29 depend from Claim 22 and therefore are patentable for at least the reasons provided for Claim 22. Based on those reasons, Applicants request reconsideration and withdrawal of the rejection of Claims 23-29.

Moreover, Claims 6, 13, 20, and 28 recite, wherein said reconfiguration logic also comprises "a respective multiplexer for each memory cell of said functional input shift register for

selecting between a respective memory cell and a respective functional input pin" based on the mode signal (Claim 6), user selector (Claim 13), the test mode (Claim 20), or the test mode selected (Claim 28). The MUX 146 of Motika, cited in the Office Action, as teaching the recited multiplexer, is not for each memory cell of LFSR 12. Therefore, Motika fails to teach the recited limitation. Omura fails to remedy the deficiency of Motika. Therefore, Applicants request further reconsideration and withdrawal of the rejection of Claims 6, 13, 20, and 28.

Moreover, Claims 7, 14, and 21 recite, "a protocol unit" coupled to the mode signal (Claim 7) or the user selector (Claims 14 and 21) and "comprising a first test sequence used for said tester of said first pin capacity and a second test sequence used for said tester of said second pin capacity". Motika teaches that the WRP patterns are generated by the tester externally to the DUT and loaded via the shift register inputs (SRIs) into the chip's shift register latches (SRLs). Col. 4, lines 63-66. Applicants note that the global weight set select register 138 (cited in the Office Action as teaching this protocol unit) fails to teach the first and second test sequences. Omura fails to remedy the deficiency of Motika. Therefore, Applicants request further reconsideration and withdrawal of the rejection of Claims 7, 14, and 21.

CONCLUSION

Claims 1-29 are pending in the present Application. Reconsideration and allowance of these claims is respectfully requested.

If there are any questions, please telephone the undersigned at 408-451-5907 to expedite prosecution of this case.

Respectfully submitted,

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